

Chip-to-chip interconnect integration technologies

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Abstract: With continuous increase in the off-chip bandwidth requirements, conventional interconnection methodologies are quickly becoming incapable of meeting the demand. Recent progress in silicon interposer and 3D integration technologies seek to alleviate some of these bottlenecks. This paper reviews the evolution of conventional interconnect methodologies and recent progress in platforms allowing high-bandwidth low-energy chip-to-chip communication.

Keywords: interconnect, nanophotonic integration, flexible interconnects, heterogeneous integration

Classification: Electron devices, circuits, and systems

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1 Introduction

Improving performance of computing systems is becoming increasingly difficult and complex as transistor scaling becomes technically and economically challenging as well as interconnects become a critical bottleneck limiting the enhancement of system performance. Conventional methods of interconnections are becoming incapable of keeping up with the high-bandwidth density requirements of next generation computing systems. Consequently, there are significant ongoing research efforts aiming to overcome this hurdle. While building reticle-sized chips can partially solve the problem, it is not economically feasible [1]. Recent advances in 2.5D [2, 3] packaging as well as silicon interposer-level optical interconnects [4] have allowed high-bandwidth communication between chips (or stack of chips) on interposers. Similarly, 3D integration [5] has been widely explored to mitigate the interconnect latency and to improve bandwidth density between stacked dice. These new approaches, however, present a unique set of challenges that needs to be addressed for effective utilization and adoption of the technology.

This paper discusses various interconnection methodologies currently being used for chip-to-chip interconnects; it then introduces some of the emerging technologies that enable high bandwidth communication between dice. The critical challenges in some of these interconnection approaches are then highlighted and an alternate system platform, leveraging flexible interconnects and self-alignment structures, is then presented. The presented platform enables integration of electrical and nanophotonic interconnects allowing high-bandwidth low-energy communication beyond the physical size of the interposer. Based on the discussion, future directions and conclusion are then presented.

2 Interconnect methodologies and challenges

2.1 Current methodologies

Motherboard based interconnects (Fig. 1(a)) have been widely used for relatively long range (\sim 30–100 cm) [6] interconnects between modules. However, with the required I/O bandwidth between chips and modules increasing drastically, mother-

board based electrical interconnects have not been able to keep up with the bandwidth demand. This is primarily because of the inherent limit of the minimum channel pitch achievable on the motherboard; high density differential stripline pair has typically pitch in the order of $\sim 600 \mu\text{m}$ [6]. Assuming 10 Gb/s channel data rate would imply that the bandwidth density achievable utilizing motherboard based electrical interconnects is in the order of $\sim 16 \text{ Gb/s/mm}$. Operating channels at a higher frequency can result in a higher aggregate bandwidth between modules, however, higher channel frequencies are limited by channel dispersion limits, the need for higher number of equalization taps and a consequent increase in the power dissipation [7]. Fig. 1(b) shows flex connectors as an alternate to connecting package modules via motherboard. High speed connectors are used to directly connect the package substrate thereby bypassing the conventional socket and motherboard. This can allow 3 \times increase in raw bandwidth and the ability to transmit higher data rates over longer distances as compared to FR4 boards [8].

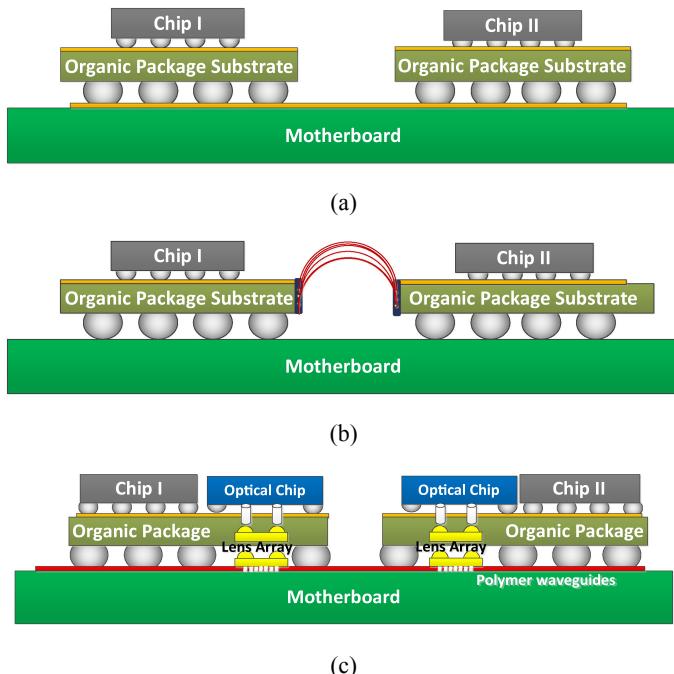


Fig. 1. Conventional interconnect methodologies (a) electrical interconnects on motherboard, (b) flex electrical connectors, and (c) optical interconnects on motherboard

Optical interconnects have also been explored for low-loss long-range chip-to-chip interconnects. The ability to send multiple wavelengths in the same channel using wavelength division multiplexing (WDM) allows higher bandwidth communication between modules. However, incorporating the electrical to optical conversion overhead and the laser efficiency increases the total energy per bit (EPB) expensed and hence limits their utilization for short distances for which electrical interconnects expense less overall energy. Furthermore, the pitch of the waveguides on the board is typically fabrication limited and hence cannot be scaled to very fine

dimensions. Fig. 1(c) shows the schematic of terabus architecture with polymer waveguides at the board level fabricated at a 62.5 μm pitch [9, 10]. A silicon based ‘optical chip’ converts the electrical signals to optical signal which is then relayed to the motherboard via a lens array and optical couplers. The terabus has been shown to provide a bidirectional aggregate data rate of 360 Gb/s bandwidth over 24 transmitter and 24 receiver channels with polymer waveguide on the optical printed circuit board (PCB) with each channel operating at 15 Gb/s and a link EPB of 9.7 pJ/bit [10]. This translates to a bandwidth density of $\sim 240 \text{ Gb/s/mm}$.

2.2 Emerging methodologies

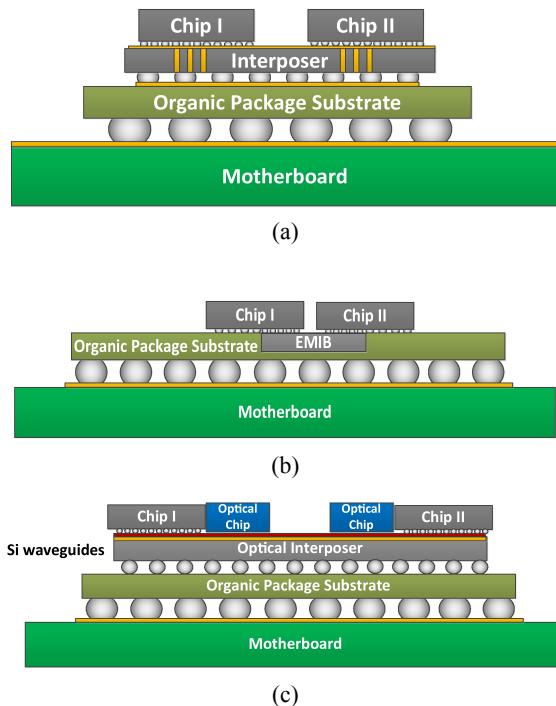


Fig. 2. Silicon based (a) electrical interposer, (b) EMIB and (c) optical interposer – fine pitch wires and waveguides achievable on silicon enables high density communication

In recent years, silicon interposers (Fig. 2(a)) have been extensively explored for various benefits including higher bandwidth density, heterogeneous integration and reduction in form factor [2]. Dense wiring on silicon interposers allows higher aggregate bandwidth between chips. Assuming a stripline differential pair pitch of 22 μm [11] for interconnect on silicon interposer and channel data rate of 10 Gb/s, the bandwidth density achievable is $\sim 450 \text{ Gb/s/mm}$. The energy efficiency of such a link of length 4 cm is 5.3 pJ/bit [11]. While EPB is lower than the optical PCB case discussed earlier, the EPB for interposer based interconnects is a strong function of length and would quickly surpass that of the optical PCB case for longer interconnects. Based on the 2.5D integration platform, there have also been different topologies presented leveraging the key benefits of the interposer technology while addressing cost, energy or packaging challenges. For example, the Intel’s embedded multi-die interconnect bridge (EMIB) packaging [3], shown in

Fig. 2(b), reduces the overall silicon area on package (compared to using a silicon interposer) and reduces the overall cost when compared to conventional interposer technology.

Integration of nanophotonic to form optical interposer (Fig. 2(c)) has also been widely researched as it allows a significantly higher bandwidth density using fine pitch silicon waveguides [1, 4] and WDM. Assuming a waveguide pitch of 10 μm [12] with 8 WDM channels and each channel operating at 10 Gb/s, the bandwidth density achievable using nanophotonics integration on interposer is $\sim 8 \text{ Tb/s/mm}$. This is clearly a lucrative option. However, again, the EPB expensed in electrical to optical conversion and vice versa, along with the laser efficiency dictates the interconnect length after which utilization of nanophotonic interconnect becomes feasible in terms of power dissipation. Oracle's macrochip [1, 13] architectures aims to leverage silicon nanophotonic integration to form a large passive grid of silicon waveguides embedded in a silicon lattice; the LSI chips (processors, RAM modules etc.) are connected to the lattice via a 'bridge' chip that converts the electrical signal to optical and couples it into the waveguide network [13, 14]. The proposed architecture can potentially operate at very low EPB (including laser power) and can enable high bandwidth communication between chips using WDM [15]. In [16], Thacker et al. demonstrate an all-solid-state WDM link with energy efficiency of 4.23 pJ/bit.

Heterogeneous 3D integration has also been widely explored to overcome bandwidth and energy challenges for LSI chips. Details on some of the recent progress in 3D integration can be found in [5, 17, 18]. Stacking of LSI chips reduces the footprint and decreases the interconnect length allowing high bandwidth density interconnects between chips. However, large scale adoption has been limited by numerous challenges including bonding and thermal concerns [18, 19, 20].

3 Silicon-bridged multi-interposer system for high bandwidth density (BWD) low energy per bit (EPB) interconnects

2.5D and 3D integration technologies discussed earlier enable high-bandwidth low-energy communication between chips. However, both have shortcomings and some trade-off is necessary in lieu of the benefits that the technology brings. While the EMIB technology enables high-bandwidth communication between chips connected via the bridge, it increases the package complexity and substrate processing. Furthermore, EMIB technology is specific for chips that are spatially in close proximity in the package and high density communication is only between the adjacent chips in the package. Moreover, since the platform doesn't currently support optical communication, it cannot take advantage of WDM to achieve higher aggregate bandwidths.

Oracle's macrochip vision portrays an aggressive target allowing high bandwidth low energy communication between chips that are even spatially further away. However, the assembly and packaging of large silicon lattice with embedded VLSI chips may pose a number of challenges that need to be overcome before the system can be realized. Furthermore, as optical communication is feasible for

relatively longer distances, the chips that are in close proximity would expense unwanted energy if only optical communication is used.

Likewise, 3D integration poses a unique set of challenges introduced by stacking chips; thermal management of stacked dice, especially with high power dice such as processors present in the stack, becomes a critical issue. Also, the wafer to wafer bonding and sequential testing of stacked dice poses additional challenges that need to be overcome before large scale adoption of the technology [18, 19, 20].

The shortcomings of these technologies are exacerbated by the fact that the number of VLSI chips needing to be integrated in a system are continuously increasing. Thus, incorporating all of these chips on an interposer would require a very large silicon interposer, which will pose mechanical handling and cost challenges. Similarly, having a 3D stack with ever increasing number of stacked chips would further amplify the current challenges. Thus, there is still a need for a large scale silicon system that allows high density electrical and optical communication between chips and extends beyond the physical limits of an interposer. The next subsection describes one approach to realize this large scale silicon system along with its enabling technologies.

3.1 System overview

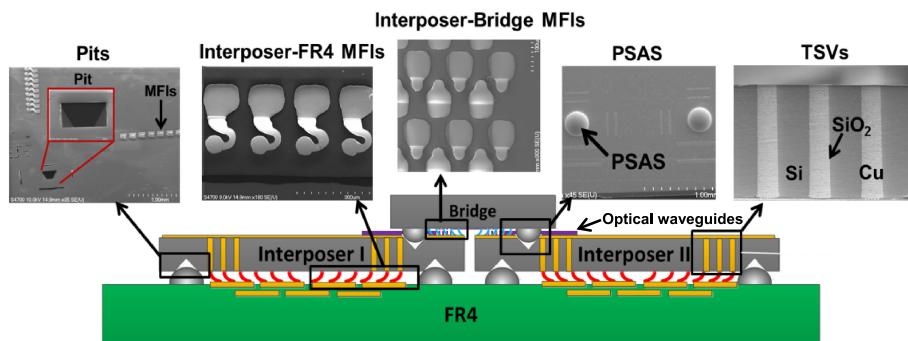


Fig. 3. Two interposer tiles mounted on FR-4 bridged using silicon

The discussion thus far motivates the utilization of interposers with electrical and optical interconnects as it can provide highest bandwidth density and efficient energy utilization compared to other methodologies discussed. It also motivates a packaging solution that allows extension of bandwidth and energy of the benefits of an interposer beyond the physical and practical limits. In this context, Yang et al. [21, 22], have proposed using silicon bridges to bridge adjacent interposer ‘tiles’. Fig. 3 shows the overview of the silicon-bridged multi-interposer system platform using a 2 tile example. The interposer tiles are directly mounted onto the FR-4 thereby eliminating package substrate; four positive self-alignment structures (PSAS) are fabricated on the FR-4 corresponding to the inverse pyramid pits on the interposer tiles to provide low-cost high accuracy alignment. Dense mechanically flexible interconnects (MFIs) are utilized to provide reliable connections to the motherboard as well as adjacent interposer via silicon bridge while overcoming coefficient of thermal expansion (CTE) mismatch and surface variations [23].

Optical waveguides can also be incorporated in the platform utilizing grating couplers to couple the light from one interposer to the other interposer via the silicon bridge. The silicon bridge allows one to extend the high-bandwidth fine pitch connections possible on an interposer beyond the physical limits of the interposer. Thus, the silicon-bridged multi-interposer system emulates a contiguous piece of large silicon allowing high density communication between interposers.

3.2 Key enabling technologies

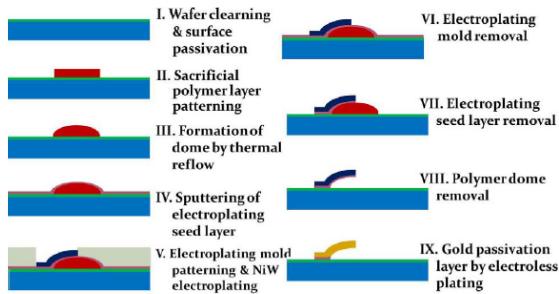


Fig. 4. MFI fabrication flow [23]

MFIs are an integral enabling technology for the realization of the system; Fig. 4 shows the fabrication flow for MFIs. The MFIs are fabricated using NiW; the higher yield strength of NiW as compared to copper [24], allows great range of elastic motion for the fabricated MFIs. The electroless gold plating passivates the MFIs and prevents any oxidation ensuring a good contact. Fig. 5 shows the optical and SEM images of the fabricated gold passivated NiW MFIs [23]. The vertical stand-off height for these MFIs is 65 μ m.

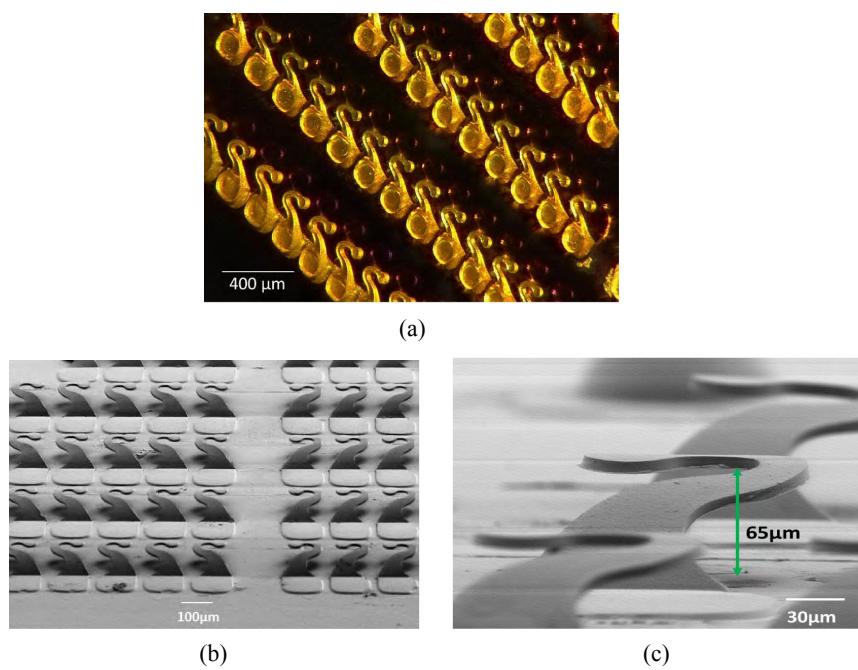


Fig. 5. (a) Optical and, (b and c) SEM images of the MFIs – vertical stand-off height is 65 μ m [23]

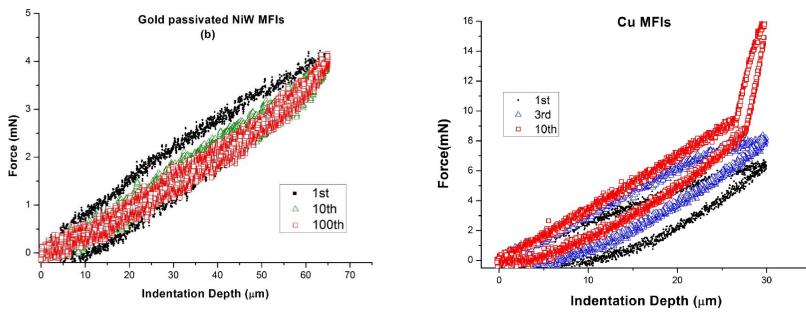


Fig. 6. Compliance measurements for gold passivated NiW and Cu MFIs [23]

Indentation tests for mechanical characterization were performed using Hysitron Triboindenter. Each cycle of indentation consisted of a downward motion, in which the indenter head deforms the MFI to a specified depth, and an upward motion in which the indenter head returns to starting height. Force – displacement graph is then plotted for the indentation cycle. Fig. 6 shows the compliance measurements performed on a single gold passivated NiW MFI along with compliance measurements of a Cu MFI. As evident from the measurements, the NiW MFIs show elastic behavior even after 100 indentations to a vertical depth of 65 μm. On the other hand, Cu MFIs quickly go into plastic deformation and loose vertical height. This can be seen from Fig. 6 where the sudden decrease in compliance at the 10th indentation can be attributed to the fact that the indenter head comes in contact with the stage on which the MFI sample is placed. These results show that the NiW MFIs can recover to original height if they, for example, go through warpage cycles in a system due to CTE mismatch. Also, the elastic behavior ensures a good electrical contact with time.

Fig. 7(a) shows the measured and simulated S11 and S21 for these MFIs. The measured loss for these MFIs at 20 GHz is ~0.3 dB; the insertion loss of a 60 μm high solder ball is ~0.1 dB at 20 GHz [25]. Although the loss of the solder ball is lower than that of the MFI, the elimination of the package layer and overcoming CTE mismatch provides significant advantages at system level. To study the rematability and effect of mechanical deformation on the electrical performance of these MFIs, three measurements were taken. An initial measurement was taken

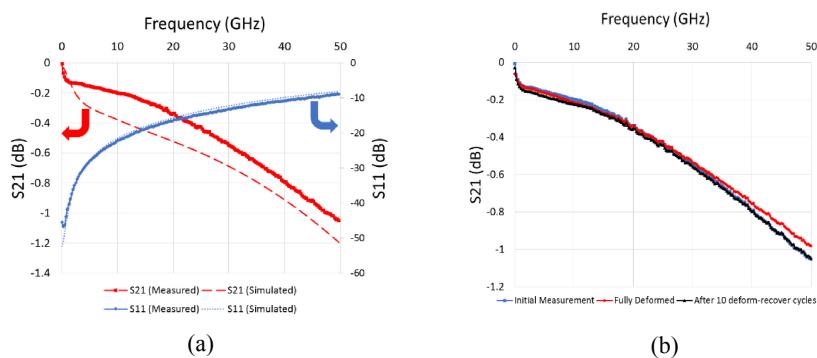


Fig. 7. (a) Measured and simulated S11 and S21 parameters for MFI, (b) comparison of S21 parameter before and after deformation cycles

without any deformation. The second measurement was taken after fully deforming the MFIs. Third measurement was performed after 10 deform-recover cycles; in each cycle, the MFIs were deformed to the full vertical range of motion and then recovered. Fig. 7(b) shows the S21 of the MFIs under the three scenarios described above. When fully deformed, the MFIs show minimal change in RF characteristics. Similarly, the effect on RF performance after 10 deform-recover cycle is negligible and the measurement after 10 deform-recover cycles matches closely to the initial measurement.

Another key enabling technology for the silicon-bridged multi-interposer system is the self-alignment utilizing PSAS and inverse pyramid pits, as shown in Fig. 8. The inverse pyramid pits are fabricated using KOH etch of silicon using nitride mask. The dimensions of the pits on both sides of the interposer are kept at $300\text{ }\mu\text{m} \times 300\text{ }\mu\text{m}$. The gap between the substrates is controlled by tuning the height of the PSAS [22]. PSAS are fabricated by precise reflow of photoresist. The PSAS-pit duo enables precise control over the gap between substrates which is a critical factor determining the optical coupling loss. The measured silicon-to-silicon and silicon-to-FR-4 alignment accuracy using vernier scale patterns is summarized in Table I. Fig. 9 also shows the profilometer scan of the fabricated PSAS. As seen from the scans, the precise reflow of the photoresist results in a perfect truncated sphere and, along with the pit, allows sub-micron alignment accuracy and precise control over the gap between substrates. As the optical coupling loss is a strong function of the misalignment [26], the submicron alignment accuracy enables low inter-layer optical coupling loss.

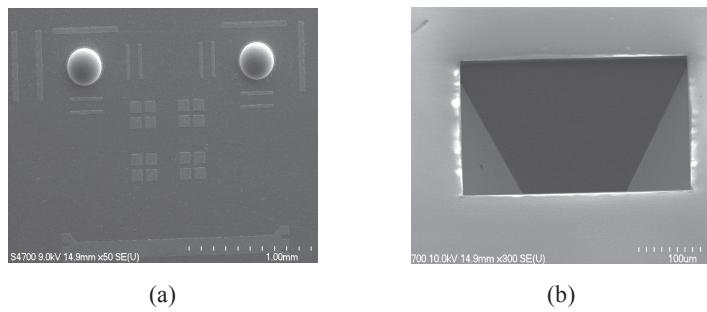


Fig. 8. (a) PSAS on bridge (b) inverse pyramid pit

Table I. Alignment accuracy (μm) using PSAS

Regions	Silicon – Silicon		Silicon – FR4	
	X	Y	X	Y
Bottom Left	<+1	<+1	+4.4	+2.0
Bottom Right	+1	+1	+3.2	-3.2
Top Left	<+1	+1	-1.6	-3.2
Top Right	<+1	<+1	-2.8	+2.4

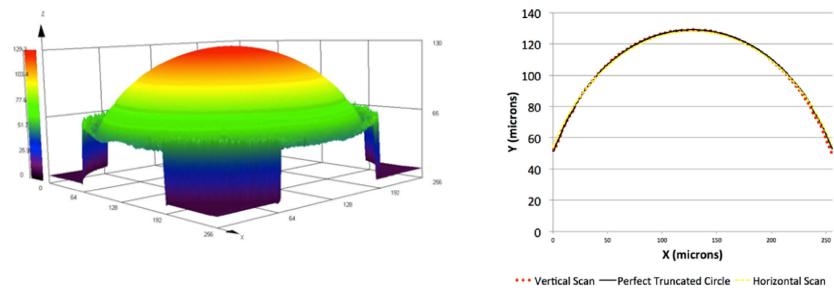


Fig. 9. Profilometer scan data for fabricated PSAS [22]

3.3 System-level analysis

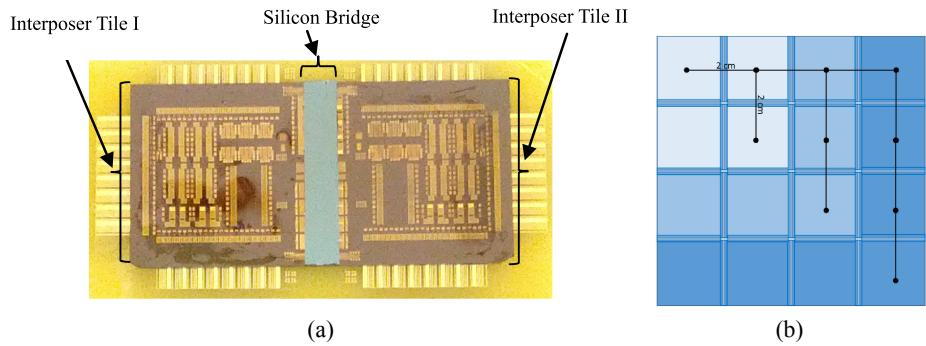


Fig. 10. (a) Assembled system with 2 interposer tiles bridged using silicon bridge (b) top view of multi-interposer system array – center to center distance between adjacent interposers is taken to be 2 cm

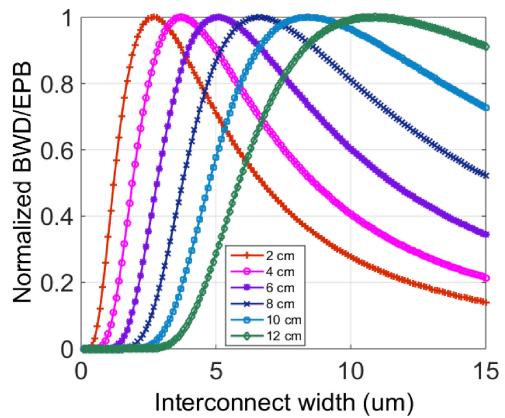


Fig. 11. Optimal width for different lengths of wires on interposers that maximizes BWD/EPB

Fig. 10(a) shows the assembled system consisting of two interposer tiles mounted directly on FR-4 and bridged using silicon bridge. The demonstrated system can be extended to have a 2 dimensional interconnected array of interposers. Top view of the different array sizes analyzed in this paper is shown in Fig. 10(b). All tiles are taken to be 2×2 cm in size and the distance between the tiles is assumed to be negligible so that the center to center distance between tiles is 2 cm. For such large scale systems, it is essential to utilize interconnection scheme that gives the highest

bandwidth at the lowest energy consumption. For the analysis that follows, the width of the electrical wire on the interposer is taken to be the one that maximizes the BWD/EPB as shown in Fig. 11. It can be seen from the figure that, for example, 2.5 μm wire width would maximize the BWD/EPB for a 2 cm long wire on interposer. Channel pitch for electrical interconnects is calculated assuming stripline structure with differential signaling and wire spacing equal to two-thirds of the width. The EPB for the electrical interconnects is calculated assuming a stripline structure with differential voltage mode signaling scheme [27]; the geometric dimensions of the transmission line are used to extract the R,L,C and G parameters; propagation constant is then determined based on these parameters. Using the receiver noise condition for a maximum BER of 10^{-12} , the minimum driving current is calculated which is then used to find the total loss in the transmission line [27].

The EPB analysis for the silicon photonic based optical interconnect has been adapted from [16]. The average transmitter and receiver electrical power is taken to be 6.93 and 4.26 mW respectively [16]. The excess loss caused by the optical couplers in the bridged interposer system is compensated by increasing the on-chip optical power to maintain a constant BER of 10^{-12} . The wall plug efficiency of the laser is taken to be 9.5% [28] and the coupling loss is assumed to be 1 dB. The EPB for electrical transmission lines is a strong function of the interconnect length. Silicon photonic based interconnects' EPB is dominated by the fixed overhead from transmitter and receiver. The silicon-bridged multi-interposer system is different from other large scale optically connected systems in the fact that each tile hop

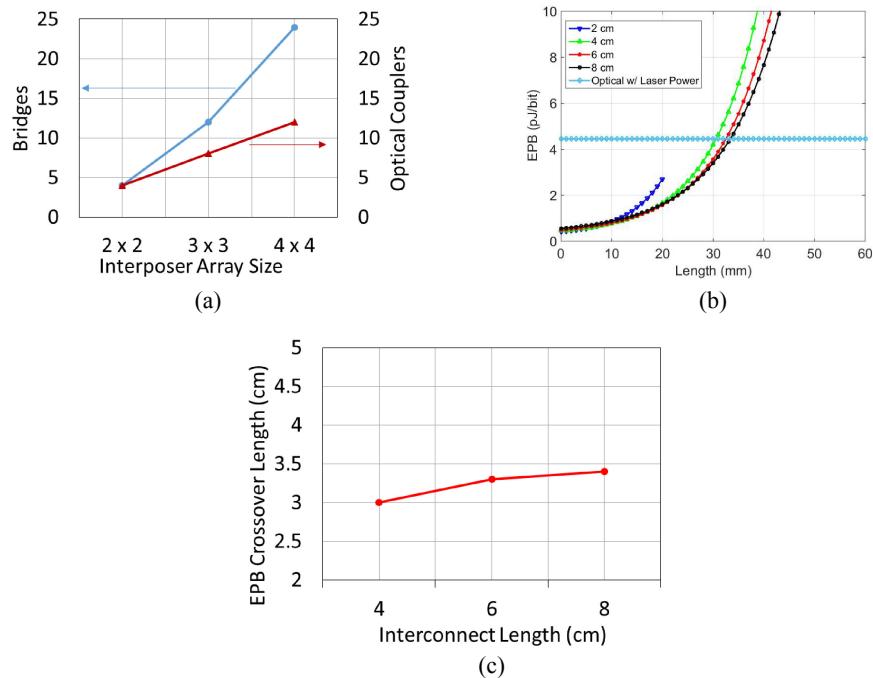


Fig. 12. (a) Number of optical couplers and silicon bridges with array size, (b) EPB comparison of four different lengths' electrical interconnects with optical interconnect and (c) crossover length – interconnect length after which electrical interconnect link dissipates more energy after this length

requires 2 optical couplings. The number of optical coupler pairs in the longest link, along with the number of bridges in the system as a function of interposer array size is shown in Fig. 12(a). Fig. 12(b) shows the EPB of electrical interconnects on silicon-bridged multi-interposer system for 4 different lengths, along with the EPB of optical interconnect. The width of each of these interconnects is taken to be the optimized width that maximizes the BWD/EPB metric (Fig. 11). Fig. 12(c) also shows the crossover length after which the electrical interconnects on interposer would expense more EPB than the silicon photonic interconnects as a function of total interconnect length. As seen from the figure, EPB line for 2 cm long electrical interconnect does not surpass that of the optical interconnect; For a case where the longest distance to be traversed is 4 cm (2×2 interposer array), the cross over length is ~ 3 cm. Hence, based on above set of assumptions, any electrical interconnect below this length would expense less EPB when compared to the silicon photonics based interconnect. It can also be seen that the cross over length remains almost unchanged for longer length. Thus, for silicon bridged systems where high bandwidth communication is required for over 3 cm distance, silicon photonics based interconnects may provide a lower energy alternate to electrical interconnects.

4 Conclusion

With the perpetual increase in bandwidth requirements of chip-to-chip communication, it is imperative that an all encompassing solution be devised – one that allows high-bandwidth low-energy communication for both short and long reach interconnects. Conventional interconnects through the motherboard suffer from coarse channel pitch and the need for higher equalization taps for longer range. While flex-based interconnects bypass the package and motherboard, the channel pitch still limits the bandwidth density achievable. Optical interconnects at motherboard level are a promising alternate, however, the relatively coarse waveguide pitch and added package complexity makes them less attractive. Silicon interposer based electrical interconnects allow high-bandwidth communication owing to the fine pitch achievable. However, long fine pitch wires on silicon quickly become very lossy and expense very high EPB. This has motivated efforts in the optical interposer regime which allows ultra-high bandwidth communication owing to the fine waveguide pitch and WDM. However, as the link EPB is dominated by the transmitter and receiver loss and the laser wall plug efficiency, the silicon nanophotonic links expense far more EPB at shorter lengths than the electrical interconnects. Although having a physically large interposer allows integration of multiple chips on to the same substrate enabling high density communication, the cost and mechanical handling of such large interposer are not feasible. The silicon-bridged multi-interposer system provides a viable alternate that allows the extension of high bandwidth density of an interposer beyond the practical limits. It further enables both electrical and optical communication for short and long reach interconnects. The self-alignment technology allows sub-micron alignment accuracy that ensure low optical coupling loss which is imperative for nanophotonic link integration.

With the demand for off-chip bandwidth projected to continue to grow, large scale silicon systems, like the silicon-bridged multi-interposer system, are likely to come into more and more use. It is also foreseeable that coexistence of electrical and nanophotonic interconnects would be critical in achieving low energy interconnects for short and long reach chip-to-chip interconnects.

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